

Call for Papers - EXTENDED

Advanced Packaging Conference (APC)

Technology trends – what’s new, what’s missing, what’s next

13-14 November 2018 / Munich Germany

Co-located with  electronica

Advanced packaging as indispensable part of the final electronic product is facing new challenges in achieving required higher performance, smaller form-factor, higher reliability levels and lower cost. This is driven by a continuously increasing number of new applications for instance in the field of IoT with integrated sensor and MEMS; different types of 5G connectivity solutions and mobile communication infrastructure; Automotive electronics for engine and transmission, chassis, safety, driver assistance, passenger comfort and infotainment; faster datacenters with more memory for big data; more space for battery and display in next generation mobile phones; the next generation imaging and image recognition systems in mobile devices; power electronics; processing cryptocurrency; and many others.

Can existing packaging technologies be extended to meet the requirements? Are new packaging technologies needed, and if yes, who will drive the development of those? Will next generations of advanced packaging and test be done by IDMs and Foundries instead by OSATs? What is done to get Wafer-Level Chip-Scale Packaging, Fan-Out Wafer-Level Packaging, Heterogenous Integration, System-in-Package and 3D Packaging ready to answer to those new challenges? The experts of Semiconductor Wafer FABs and IDMs (Frontends) and Packaging, Assembly and Test in OSATs, Test Houses and IDMs (Backends) need to move closer together, new high sophisticated functional materials need to be developed and tested for higher system robustness, new more powerful inspection methods are needed to ensure the quality level required, and flexible multi-temperature test concepts need to be developed. At this year’s Advanced Packaging Conference, we want to present the latest advancements and innovations in this field. If your company is active in packaging as well as advanced packaging and test, we invite you to submit an abstract.

Papers should cover packaging, assembly and test process, and volume manufacturing challenges for:

Packaging/ Assembly

- Heterogeneous Integration / System in Package;
- MEMS and Sensor integration;
- Optoelectronics and Photonics Packaging;
- High Voltage and Power Packaging
- Chip embedding Packaging Technologies;
- Wafer-Level Packaging;
- Merge of Frontend- and Backend technologies;
- Move from wafer scale to panel scale packaging
- Chip-Package-Interaction, Modeling
- Parallel processing solutions, scalability and manufacturing on large format;
- Additive assembly technology
- Thin wafer/ panel handling;
- Interconnect technologies for improved performance and reliability;
- The role of material, and material development for higher reliability;
- Higher yield/MSL-level in SiP modules by new materials
- Process development and control;
- Quality and reliability assurance;
- Metrology and inspection methods;
- Failure modes and analysis.

Wafer/ Package Test:

- Wafer-Level Package handling and test;
- Alignment for small contact pitches;
- Overcoming packaging limits to enable test at high parallelism;
- Packaging and test: strategies for high-energy alpha wave sensitive materials;
- Validation of interconnects at multiple temperatures (room, hot and cold);
- Validation of interconnects at high power (high voltage and/or current);
- Validation of interconnects at microwave frequencies.
- Contactless testing
- Handling and testing unusual packages and modules
- Test strategies for multi-chip packages
- Testing packages with integrated sensors

Instructions to submit an abstract – To submit your abstract please click [here](#).

General guidelines:

- Please submit your abstracts, biography and a photo via internet until **18 May 2018**. Abstracts submitted via fax, e-mail, post, or other methods will generally not be accepted.
- The conference language is English.
- The abstract should have between 1.000 and 2.000 characters (Starting with descriptive paragraph identifying issue addressed and solution). Please focus on the news instead of describing state-of-the-art.
- Abstract modifications, changes and corrections will be accepted until the 18 May 2018.

Your presentation may not be included in the review process unless the information is complete.

Evaluation criteria include significance, usefulness for the manufacturing world and clarity and accuracy as a paper. Abstracts will be peer-reviewed and selected relative to the points above. We encourage application related presentations, i.e. on joint projects between users and suppliers. Papers are to be non-commercial and focus on the technical/economical merits of a process rather than the individual company's product benefits.

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| Deadline: | Submit your abstracts and biography until <u>18 May 2018</u>. |
| Changes: | After your first registration your data are saved and can be modified until 18 May 2018 . |
| Notification: | Selected presenters will be notified by 20 July 2018. |

SEMI Europe Advanced Packaging Conference (APC) Committee:

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| Mehmet Akcıt, Hesse-Knipps | Jens Mueller, IMAPS Europe Chapter |
| Rolf Aschenbrenner, Fraunhofer IZM | Pascal Oberndorff, NXP |
| Peter Cockburn, Xcerra Corporation | Thomas Oppert, Pac Tech |
| Ivan Galesic, OSRAM Opto-Semiconductors | Amandine Pizzagalli, Yole Développement |
| Michel Garnier, STMicroelectronics | Klaus Pressel, Infineon |
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| Ingo Henkel, Bosch | Roland Rettenmeier, Evatec |
| Graham Jones, CMT Semiconductor Services | Reinhart Richter, EBARA PM Europe |
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| Frank Kuechenmeister, GLOBALFOUNDRIES | Gilles Simon, CEA-Leti |
| Andy Longford (co-chair), Panda Europe | |

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