Call for Abstracts - EXTENDED

Advanced Packaging Conference (APC)

Packaging & Test - Challenges Towards High Reliability

12-13 November 2019 / Munich Germany

Co-located with productronica

With the advent of IoT, Autonomous Driving and Smart Everything the semiconductor industry is undergoing ever closer integration between the fields of More Moore and More Than Moore. The spiraling costs of transistor scaling are leading to highly inventive and challenging applications enabling improved PPAC (Power, Performance, Area, Cost), closer integration with alternative device types plus the need to bring Edge Computing into the local area compute arena. With all of these new integration and device approaches, Advanced Packaging continues to become a key enabler for the continued growth of our industry.

The scientific and engineering difficulties brought about by ever increasing complexity in terms of materials, equipment and metrology development also begin to lead us towards the introduction of Artificial Intelligence (AI) methodologies at package level to maintain high yield towards maximum value products. As a result package and device reliability, materials characterization, data capture and interpretation all become key areas of research for an ever more connected environment.

Wafer-Level Chip-Scale Packaging, Fan-Out Wafer-Level Packaging, Heterogenous Integration, System-in-Package and 3D Packaging are all areas of research maturing into mass production capable offerings. In order to enable this IDM, OSATs and foundries are developing business models to enable faster time-to-market (low cost) packages and the continuous improvement of those packages is a critical research area. At this year's Advanced Packaging Conference, we want to present the latest advancements and innovations in this field. If your company is active in packaging as well as advanced packaging and test, we invite you to submit an abstract.

Papers should cover packaging, assembly and test process, and volume manufacturing challenges for:

Packaging/ Assembly

- Heterogeneous Integration / System in Package;
- MEMS and Sensor integration;
- Optoelectronics and Photonics Packaging;
- High Voltage and Power Packaging;
- Chip embedding Packaging Technologies;
- Wafer-Level Packaging;
- Merge of Frontend- and Backend technologies;
- Move from wafer scale to panel scale packaging
- Chip-Package-Interaction, Modeling;
- Thin wafer/ panel handling;
- Interconnect technologies for improved performance and reliability;
- The role of material, and material development for higher reliability;
- Higher yield/MSL-level in SiP modules by new materials;
- Process development and control;
- Quality and reliability assurance;
- Metrology and inspection methods;

• Parallel processing solutions, scalability and manufacturing on large format; • Additive assembly technology;	• Failure modes and analysis; • Cost reduction of advanced packaging.
Wafer/ Package Test: ▪ Wafer-Level Package handling and test; ▪ Alignment for small contact pitches; ▪ Overcoming packaging limits to enable test at high parallelism; ▪ Packaging and test: strategies for high-energy alpha wave sensitive materials; ▪ Validation of interconnects at multiple temperatures (room, hot and cold); ▪ Contactless testing;	▪ Validation of interconnects at high power (high voltage and/or current); ▪ Validation of interconnects at microwave frequencies; ▪ Handling and testing unusual packages and modules; ▪ Test strategies for multi-chip packages; ▪ Testing packages with integrated sensors; ▪ Using big data analytics from test to optimize packaging process.

Instructions to submit an abstract – To submit your abstract please click here.

General guidelines:

- Please submit your abstracts, biography and a photo via internet until **24 May 2019**. Abstracts submitted via fax, e-mail, post, or other methods will generally not be accepted.
- The conference language is English.
- The abstract should have between 1.000 and 2.000 characters (Starting with descriptive paragraph identifying issue addressed and solution). Please focus on the news instead of describing state-of-the-art.
- Abstract modifications, changes and corrections will be accepted until the 24 May 2019.

Your presentation may not be included in the review process unless the information is complete.

Evaluation criteria include significance, usefulness for the manufacturing world and clarity and accuracy as a paper. Abstracts will be peer-reviewed and selected relative to the points above. We encourage application related presentations, i.e. on joint projects between users and suppliers. Papers are to be non-commercial and focus on the technical/economical merits of a process rather than the individual company's product benefits.

Deadline:	**Submit your abstracts and biography until 24 May 2019.**
Changes:	After your first registration your data are saved and can be modified until **24 May 2019**.
Notification:	**Selected presenters will be notified by 19 July 2019.**

SEMI Europe Advanced Packaging Conference (APC) Committee:

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